EE 330 Lecture 34

Layout of Current Mirrors

Common-Centroid Layouts

High Gain Amplifiers

Cascode Amplifiers

Fall 2025 Exam Schedule

Exam 1 Friday Sept 26

Exam 2 Friday October 24

Exam 3 Friday Nov 21

Final Exam Monday Dec 15 12:00 - 2:00 PM

Review From Previous Lecture

Basic Amplifier Application Gain Table

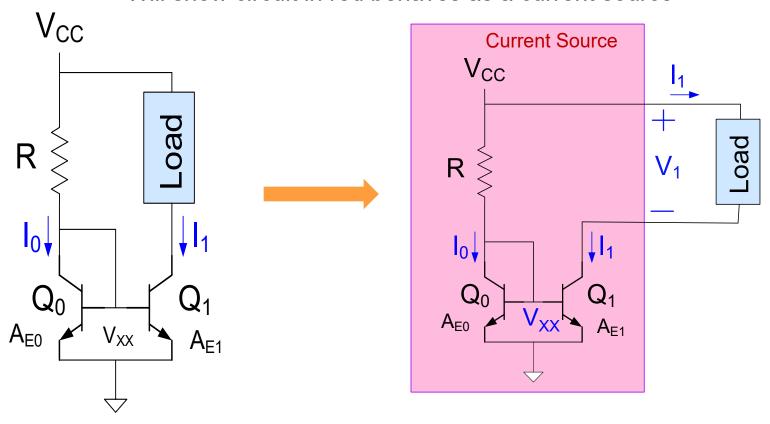
(for low-frequency operation)

	CE/CS		CC/CD		CB/CG		CEwRE/CSwRS	
	BJT	MOS	BJT	MOS	BJT	MOS	BJT	MOS
	V _{in} ⊕ R _C	v_{in}	$v_{\rm in}$	v _{in} v_{out}	v_{in}	$v_{\rm in}$	v_{in}	v_{in}
			v_{in}	$v_{\rm in}$			_	
A _V	- g _m R _C		<u>9m</u> 9 _m + 9E		$g_{m}R_{C}$		- R _C R _E	
	$-\frac{I_{CQ}R_{C}}{V_{t}}$	$-\frac{2I_{DQ}R_{D}}{V_{EB}}$	$\frac{I_{CQ}R_E}{I_{CQ}R_E + V_t}$	$\frac{2I_{DQ}R_{E}}{2I_{DQ}R_{E} + V_{EB}}$	$\frac{I_{CQ}R_{C}}{V_{t}}$	$\frac{2I_{DQ}R_{C}}{V_{EB}}$		
R _{in}	r _π		r _π +βR _E		9 _m -1		r _π + βR _E	
	$\frac{\beta V_t}{I_{CQ}}$	∞	$\frac{\beta V_t}{I_{CQ}} + \beta R_E \cong \beta R_E$	∞	$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2l_{DQ}}$	$\beta \left(\frac{V_t}{I_{CQ}} + R_E \right) \simeq \beta R_E$	∞
R _{out}	R _C		g _m -1		R _C		R _C	
	•		$\frac{V_t}{I_{CQ}}$	V _{EB} 2l _{DQ}			-	

(<u>not</u> two-port models for the four structures)

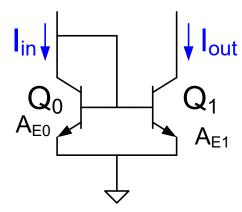
Can use these equations only when small signal circuit is EXACTLY like that shown !!

Will show circuit in red behaves as a current source



R and Q_0 simply generate voltage V_{XX} in previous circuit

But sensitivity of I_1 is much smaller than using voltage source for generating $V_{\chi\chi}$

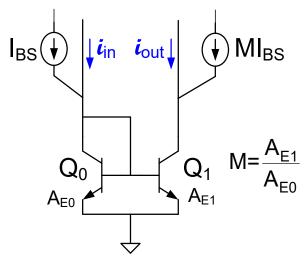


npn Current Mirror

If the base currents are neglected

$$I_{\text{out}} = \left[\frac{A_{\text{E1}}}{A_{\text{E0}}} \right] I_{\text{in}}$$

- Output current linearly dependent on lin
- Small-signal and large-signal relationships the same since linear
- Serves as a current amplifier
- Widely used circuit



npn current mirror amplifier

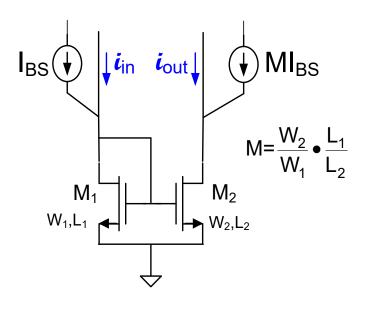
$$i_{\text{out}} = \left[\frac{A_{\text{E1}}}{A_{\text{E0}}}\right] i_{\text{in}}$$

Amplifies both positive and negative currents (provided i_{IN}>-I_{BS})

Current amplifiers are easy to build !!

Current gain can be accurately controlled with appropriate layout !!

Review From Previous Lecture n-channel current mirror current amplifier

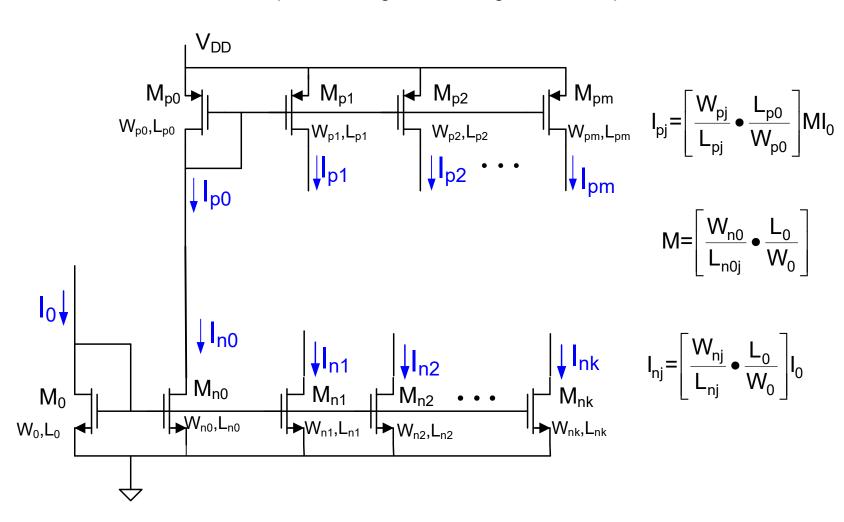


$$i_{\text{out}} = \left[\frac{W_2}{W_1} \frac{L_1}{L_2} \right] i_{\text{in}}$$

Amplifies both positive and negative currents

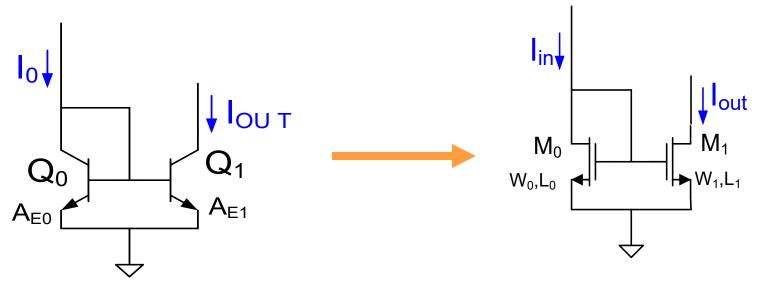
Review From Previous Lecture Current Sources/Mirrors

multiple sourcing and sinking current outputs



m and k may be different Often M=1

Current Sources/Mirrors Summary



npn Current Mirror

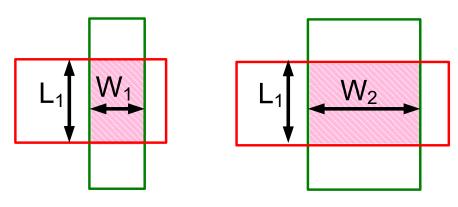
$$I_{out} = \left[\frac{A_{E1}}{A_{E0}} \right] I_{in}$$

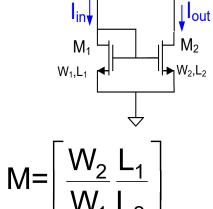
n-channel Current Mirror

$$\mathbf{I}_{\text{out}} = \left[\frac{\mathbf{W}_1}{\mathbf{W}_0} \frac{\mathbf{L}_0}{\mathbf{L}_1} \right] \mathbf{I}_{\text{in}}$$

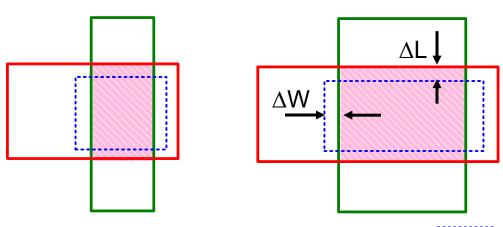
- Current mirror gain <u>can</u> be accurately controlled!
- Layout is important to get accurate gain (for both MOS and BJT)

Example with M = 2





Standard layout



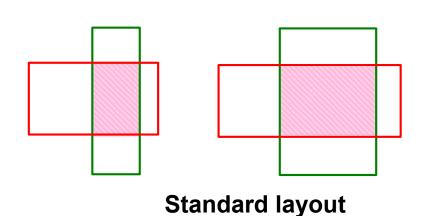
$$M = \left[\frac{W_2 + 2\Delta W}{W_1 + 2\Delta W} \bullet \frac{L_1 + 2\Delta L}{L_2 + 2\Delta L} \right]$$

$$\mathsf{M} = \left\lceil \frac{2\mathsf{W}_1 + 2\Delta\mathsf{W}}{\mathsf{W}_1 + 2\Delta\mathsf{W}} \bullet \frac{\mathsf{L}_1 + 2\Delta\mathsf{L}}{\mathsf{L}_1 + 2\Delta\mathsf{L}} \right\rceil \neq 2$$

Gate area after fabrication depicted

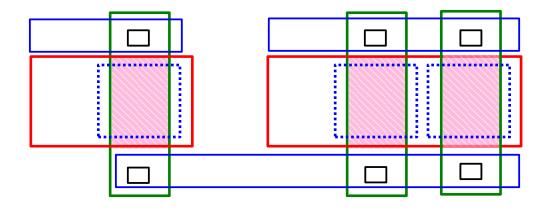
 ΔL and ΔW can be positive or negative

Example with M = 2



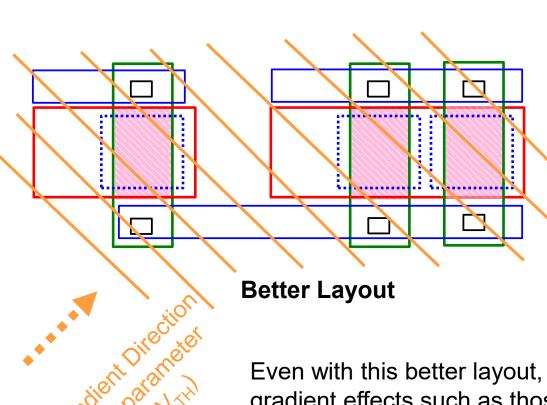
$$M = \left[\frac{W_2}{W_1} \frac{L_1}{L_2} \right]$$

$$M = \left[\frac{2W_1 + 2\Delta W}{W_1 + 2\Delta W} \bullet \frac{L_1 + 2\Delta L}{L_1 + 2\Delta L} \right] \neq 2$$



$$\mathsf{M=} \left[\frac{2\mathsf{W}_1 + 4\Delta\mathsf{W}}{\mathsf{W}_1 + 2\Delta\mathsf{W}} \bullet \frac{\mathsf{L}_1 + 2\Delta\mathsf{L}}{\mathsf{L}_1 + 2\Delta\mathsf{L}} \right] = 2$$

Example with M = 2



$$\mathsf{M} = \left[\frac{2\mathsf{W}_1 + 4\Delta\mathsf{W}}{\mathsf{W}_1 + 2\Delta\mathsf{W}} \bullet \frac{\mathsf{L}_1 + 2\Delta\mathsf{L}}{\mathsf{L}_1 + 2\Delta\mathsf{L}} \right] = 2$$

But this analysis was based upon assumption of matching of process parameters

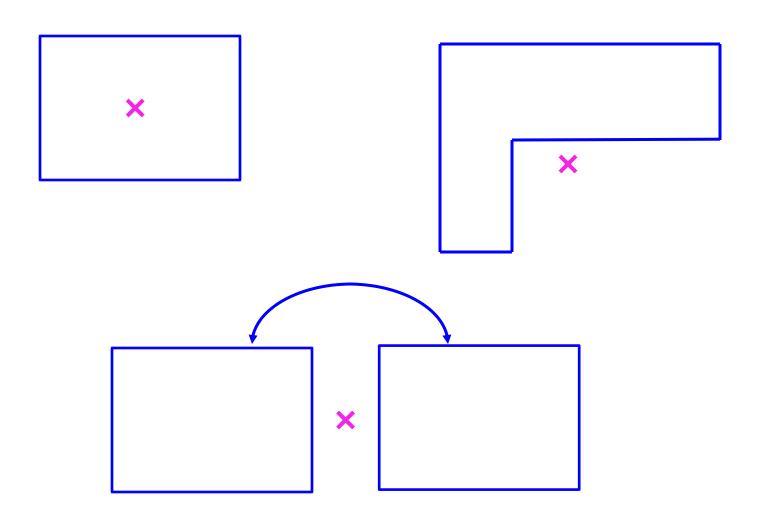
$$I_{in} = \frac{\mu_0 C_{OX} W_0}{2L_0} (V_{GS0} - V_{T0})^2$$

$$I_{out} = \frac{\mu_1 C_{OX} W_1}{2L_1} (V_{GS1} - V_{T1})^2$$

Even with this better layout, the current ratio will not be 2 if gradient effects such as those depicted here are shown

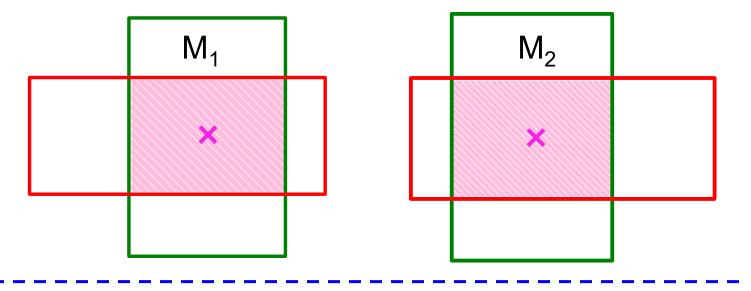
And both magnitude and direction of gradient effects are a random variable which will vary across a die

X Denotes Geometric Centroid

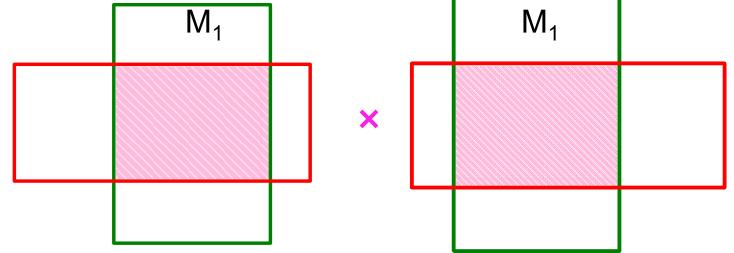


Geometric Centroids of Channel

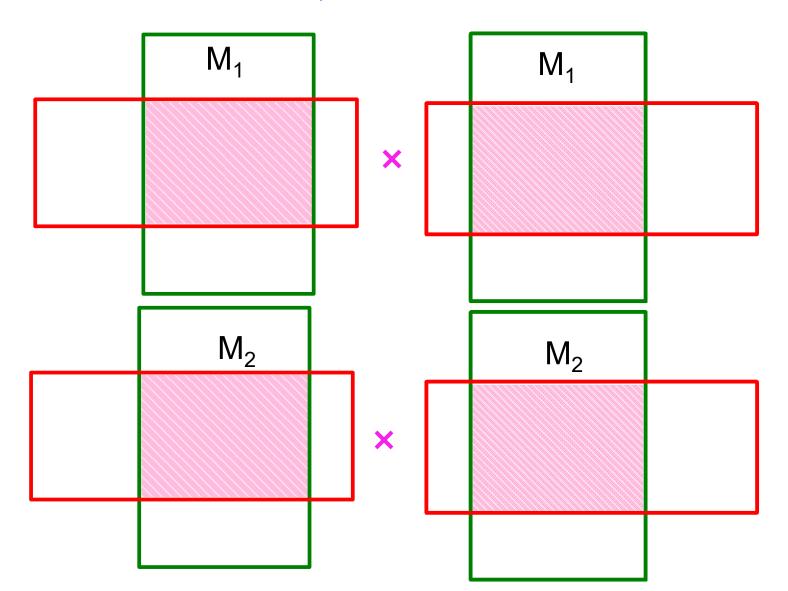
Two Transistors:



Two Parts of One Transistor:

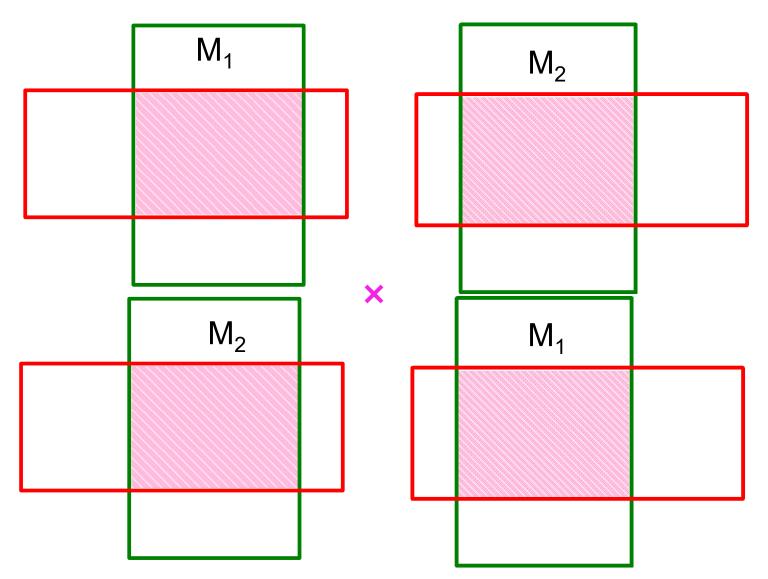


Two Transistors each with two parts:



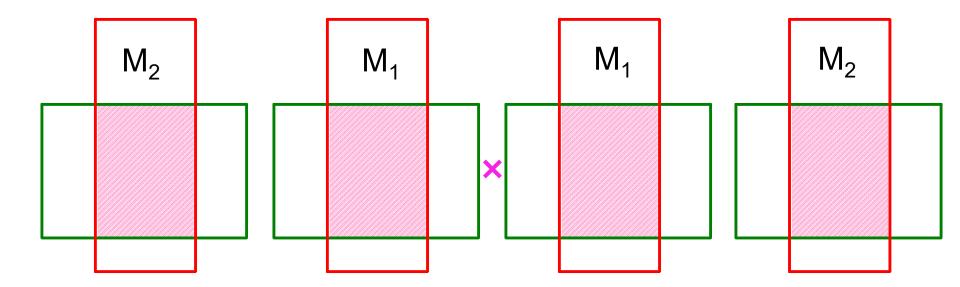
Common Centroid for Ideally Matched Devices

Two Transistors each with two parts:



Common Centroid for Matched Devices

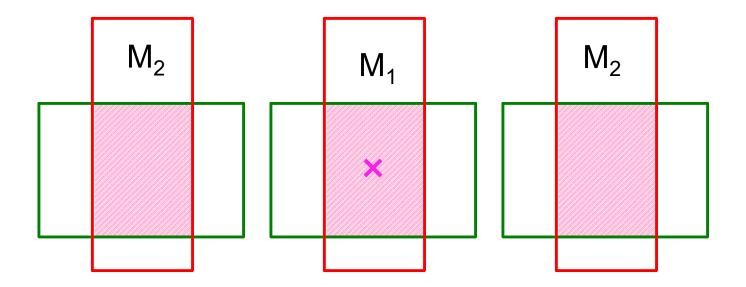
Two Transistors each with two parts:



Common Centroid for Ratioed Devices M

$$M = \frac{W_2}{W_1} \frac{L_1}{L_2} = 2$$

Two Transistors with different effective widths:



Threshold voltage dependent upon position V_{TH}(x,y) - Significant changes in threshold voltage can occur due to gradient effects - This can seriously degrade matching in

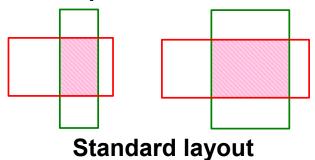
Gradients in key parameters (V_{TH}, μC_{OX})
usually nearly linear

matching-critical circuits

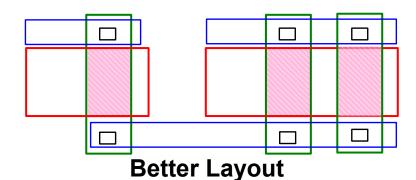
- If the threshold voltage of a transistor changes with position, it can be reasonably accurately modeled with an "equivalent" threshold voltage
 - For linear gradient, V_{THEQ}=V_{TH}(X_C,Y_C)



Example with M = 2



$$M = \left[\frac{W_2}{W_1} \frac{L_1}{L_2} \right]$$



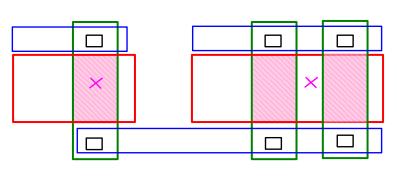
$$\mathsf{M} = \left[\frac{2\mathsf{W}_1 + 4\Delta\mathsf{W}}{\mathsf{W}_1 + 2\Delta\mathsf{W}} \bullet \frac{\mathsf{L}_1 + 2\Delta\mathsf{L}}{\mathsf{L}_1 + 2\Delta\mathsf{L}} \right] = 2$$

$$M = \left[\frac{2W_1 + 4\Delta W}{W_1 + 2\Delta W} \bullet \frac{L_1 + 2\Delta L}{L_1 + 2\Delta L} \right] = 2$$

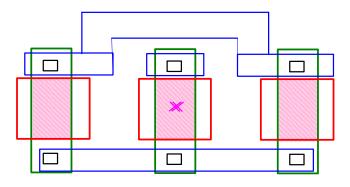
This is termed a common-centroid layout

Layout of Matching-Critical Circuits

Example with M = 2

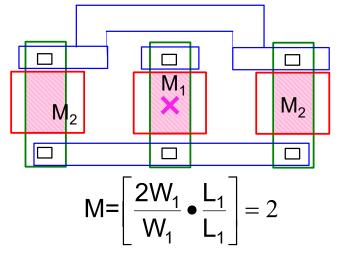


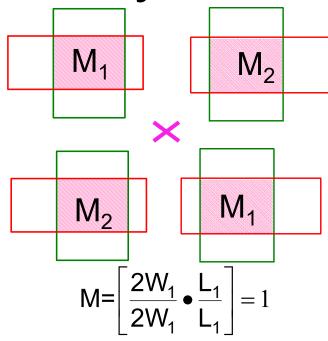




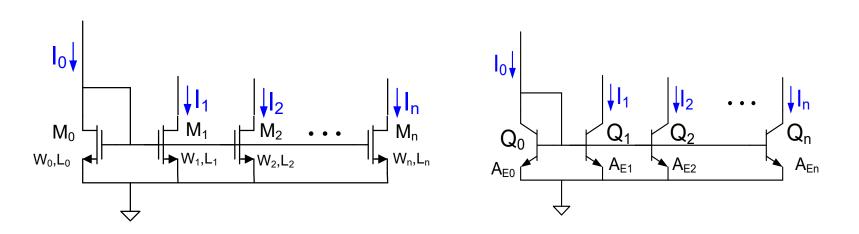
Common-centroid Layout

Theorem: Linear gradient mismatch eliminated with commoncentroid layout! Common-Centroid Layouts



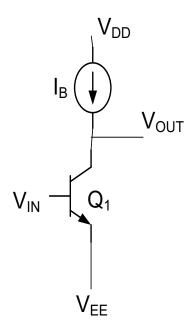


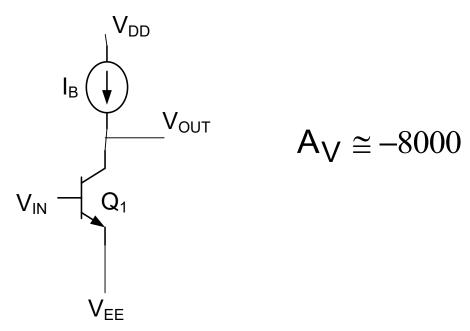
- Individual transistors in matching-critical circuits often decomposed into multiple parallel unary devices connected in parallel and placed with common centroid
- Common-Centroid layout approach widely used to minimize (ideally cancel) linear gradient effects in matching-critical circuits
- Applications extend well beyond current mirrors
- More than 2 devices can share a common centroid



If I₀ is practically generated (it can be), now have available a large number of accurate current sources or sinks that can be used for biasing and for other purposes on chip!

Will now return to discussion of high gain amplifiers





Why are we interested in high-gain amplifiers?

- High gain amplifiers typically have some very undesirable properties
 Nonlinear, gain highly dependent upon process variations and temperature, frequency response poor, noisy,
- So we can build feedback amplifiers !!

$$A_{V} \cong -8000$$

$$V_{IN} = Q_{1}$$

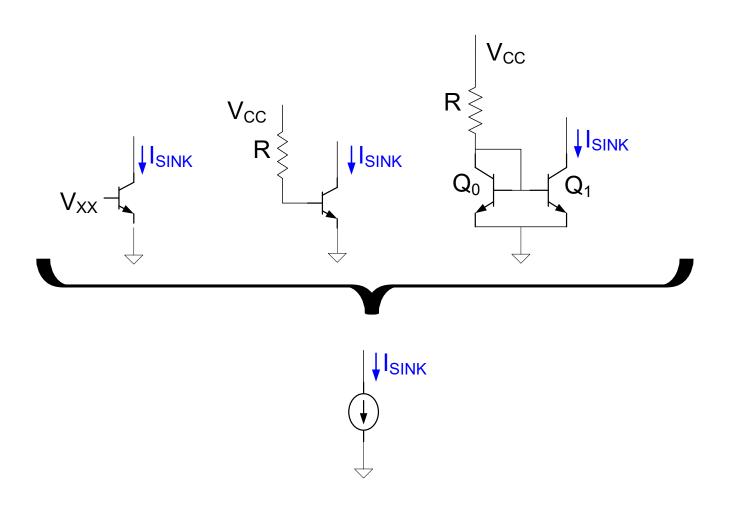
$$V_{EF}$$

How can we build the current source?

What is the small-signal model of an actual current source?

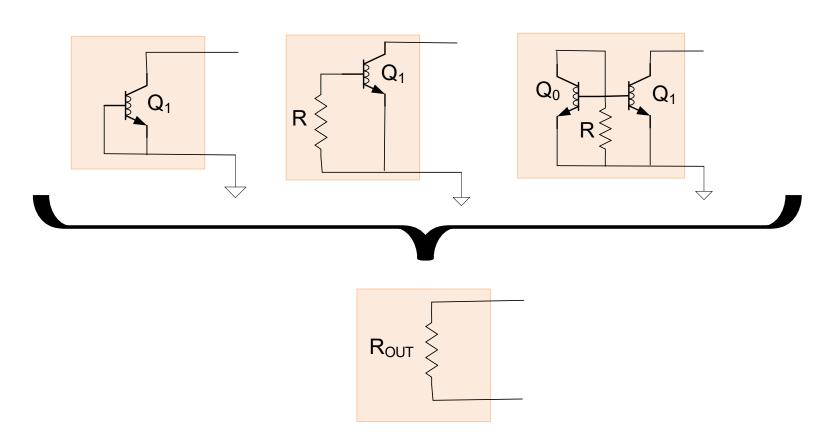
How can we build current source (or sink)?

3 of many ways shown for bipolar process



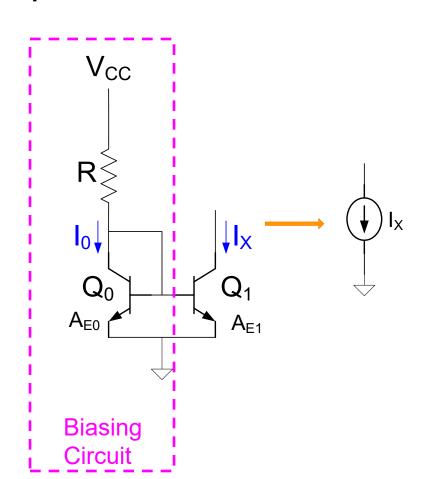
How can we build current source (or sink)?

Note: All are small-signal one-ports and equivalent to a resistor R_{OUT}

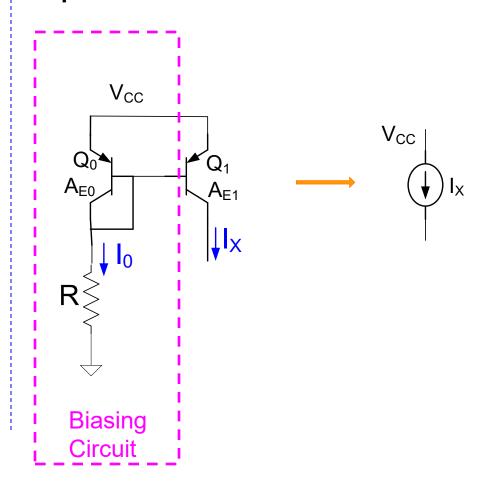


Consider as an example:

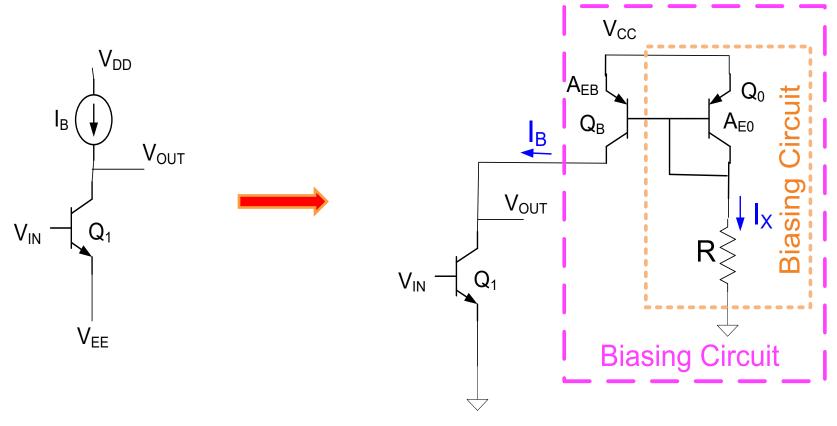
Bipolar Mirror-Based Current Sink



Bipolar Mirror-Based Current Source

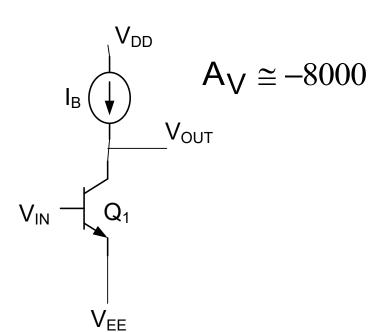


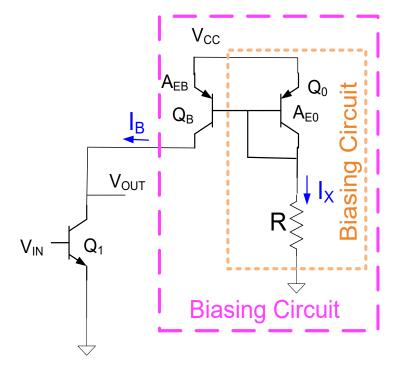
Consider as an example:



- Bias circuitry for biasing circuit requires only a single independent dc voltage source, resistor, and BJT!
- Incremental overhead for each additional current output is only one transistor, Q_B

Consider as an example:



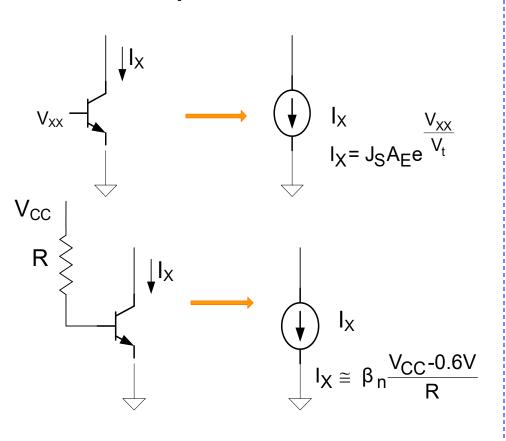


How can we build the current source?

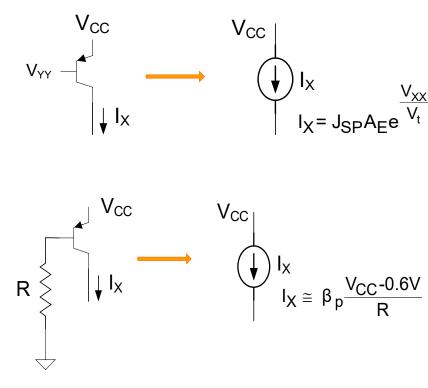
→ What is the small-signal model of an actual current source?

DC Models of Basic Bipolar Sinks and Sources

Basic Bipolar Current Sinks

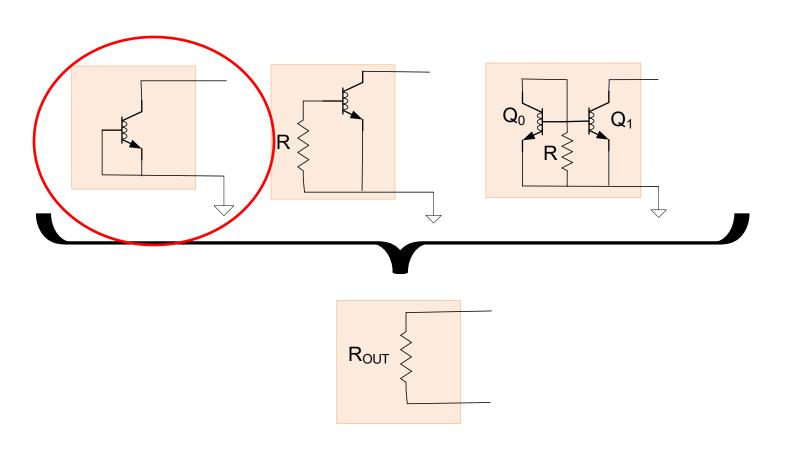


Basic Bipolar Current Sources

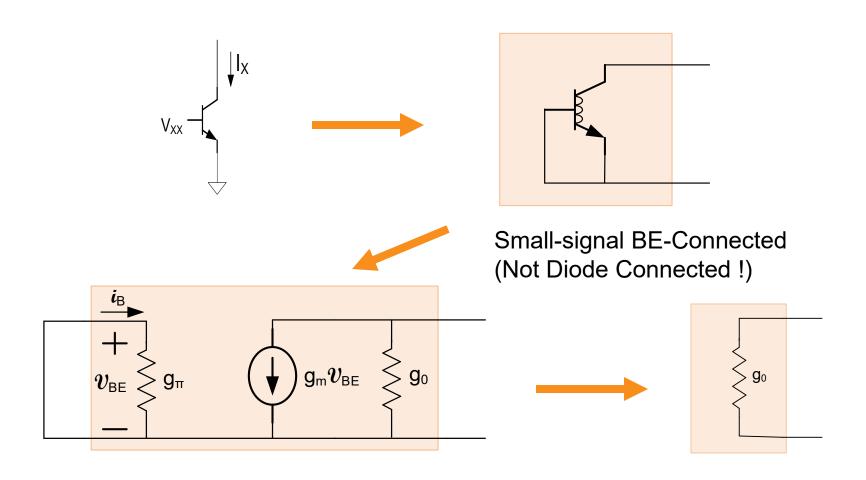


- Very practical methods for biasing the BJTs (or MOSFETs) can be used
- Current Mirrors often used for generating sourcing and sinking currents
- Can think of biasing transistors with V_{xx} and V_{yy} in these current sources

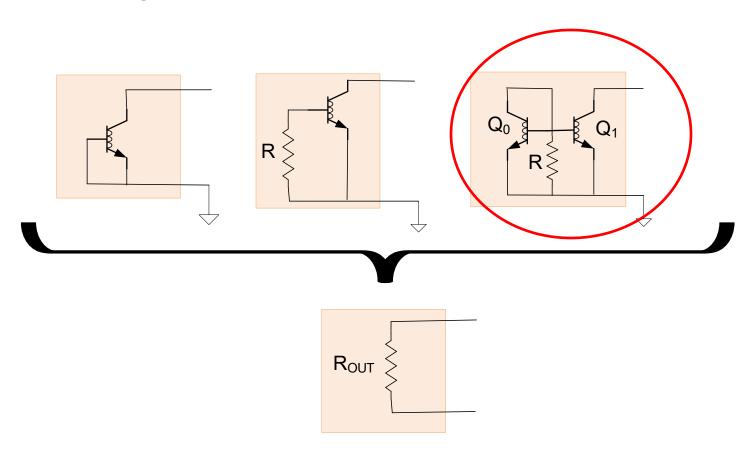
Small-signal Model of BJT Current Sinks and Sources



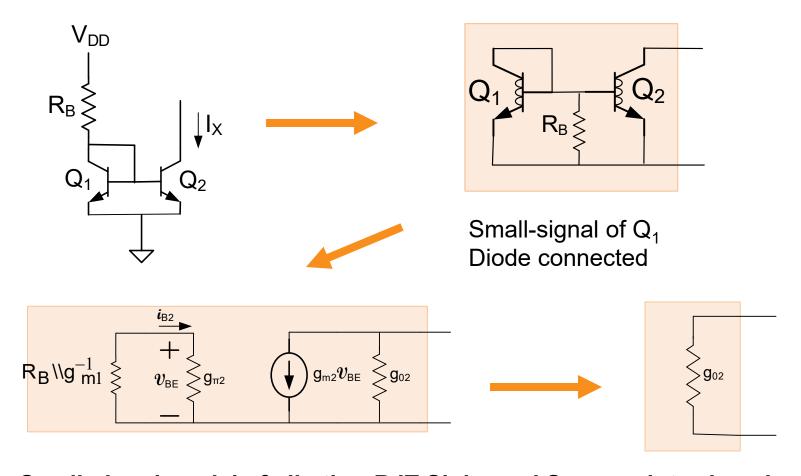
Small-signal Model of BJT Current Sinks and Sources



Small-signal Model of BJT Current Sinks and Sources



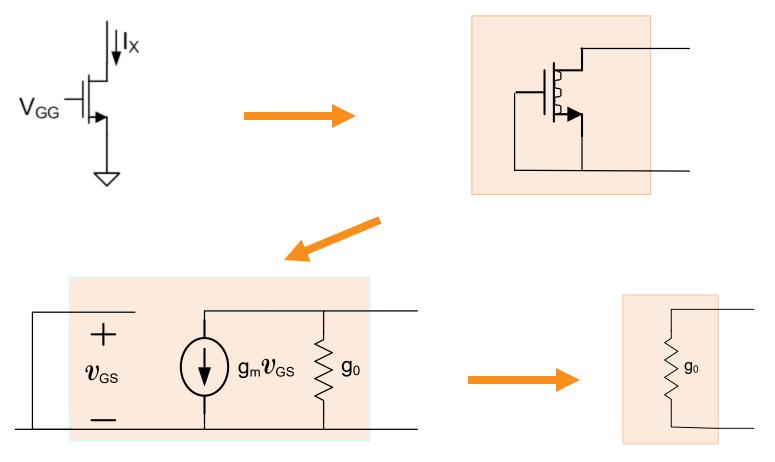
Small-signal Model of BJT Current Sinks and Sources



Small-signal model of all other BJT Sinks and Sources introduced so far are the same

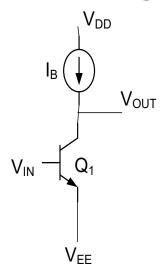
Basic Current Sources and Sinks

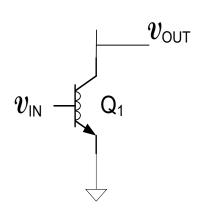
Small-signal Model of MOS Current Sinks and Sources



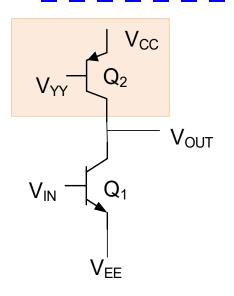
Small-signal model of all other MOS Sinks and Sources introduced thus far are the same

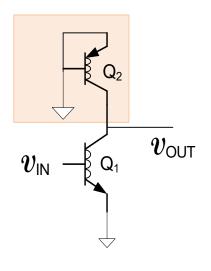
High-gain bipolar amplifier





$$A_V = \frac{-g_m}{g_0}$$





$$v_{\mathsf{IN}} + v_{\mathsf{BE1}} > \mathsf{g}_{\mathsf{m1}} + v_{\mathsf{BE1}} > \mathsf{g}_{\mathsf{m1}} + v_{\mathsf{BE1}} > \mathsf{g}_{\mathsf{m1}} + v_{\mathsf{BE1}} > \mathsf{g}_{\mathsf{m2}} + v_{\mathsf{BE1}} > \mathsf{g}_{\mathsf{m1}} + v_{\mathsf{BE1}} > \mathsf{g}_{\mathsf{m1}} + v_{\mathsf{BE1}} > \mathsf{g}_{\mathsf{m2}} + v_{\mathsf{BE1}} > \mathsf{g}_{\mathsf{m1}} + v_{\mathsf{BE1}} > \mathsf{g}_{\mathsf{m2}} > \mathsf{g}_{\mathsf{m$$

$$A_V = \frac{-g_{m1}}{g_{01} + g_{02}} \cong \frac{-g_{m1}}{2g_{01}}$$

High-gain amplifier

$$V_{DD}$$

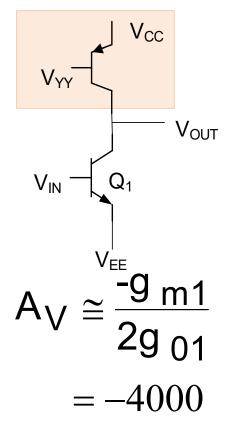
$$V_{IN} = Q_1$$

$$V_{EE} = Q_0$$

$$Q_0$$

=-8000

Recall:
$$\frac{g_{m}}{g_{0}} = \frac{g_{m1}}{g_{01}} = \frac{V_{AF}}{V_{t}} \cong 8000$$



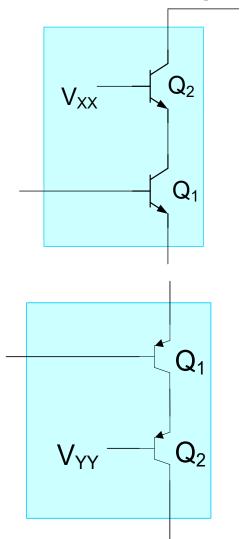
- Nonideal current source decreased the gain by a factor of 2
- But the voltage gain is still quite large (-4000)

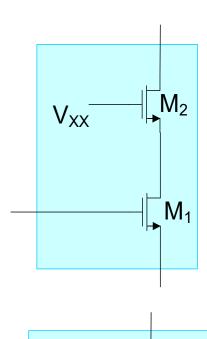
High-gain amplifier

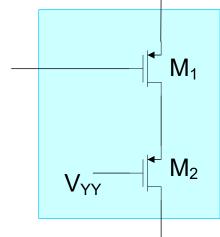
Discuss

Can the gain be made even larger?

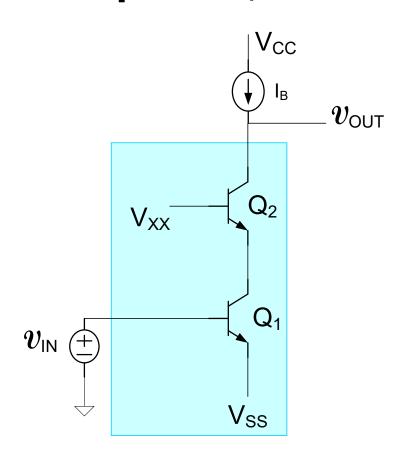
The Cascode Configuration







The Cascode Amplifier (consider npn BJT version)





- Actually a cascade of a CE stage followed by a CB stage but usually viewed as a "single-stage" structure
- Cascode structure is widely used

Basic Amplifier Structures



- 1. Common Emitter/Common Source
- 2. Common Collector/Common Drain
- 3. Common Base/Common Gate
- 4. Common Emitter with R_E/ Common Source with R_S

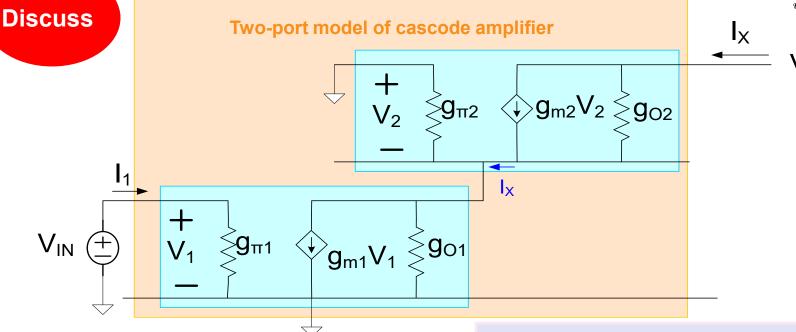


- 5. Cascode (actually CE:CB or CS:CD cascade)
- 6. Darlington (special CE:CE or CS:CS cascade)

The first 4 are most popular

The Cascode Amplifier (consider npn BJT version) $_{ extsf{-}}v_{\mathsf{out}}$ Q_2 V_{SS} I_X Q_2 $\diamondsuit g_{m2}V_2 \gtrless g_{O2}$ $\geqslant g_{\pi 2}$ Q_1 + V₁ $\leq g_{\pi 1}$





$$(V_X+V_2)g_{02}+V_2g_{m2}=I_X$$

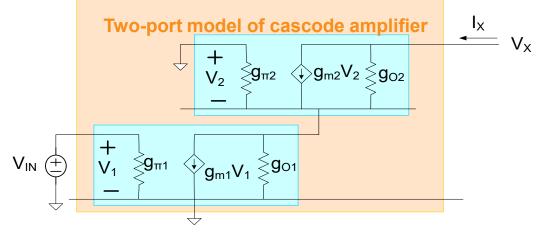
 $V_1 g_{m1}-V_2(g_{01}+g_{\pi 2})=I_X$

Standard Form for Amplifier Two-Port

Observing V₁=V_{IN} and eliminating V₂ between these two equations, we obtain

$$V_{IN} = I_{1} \bullet \frac{1}{g_{\pi 1}}$$
 and
$$V_{X} = I_{X} \bullet \left[\frac{g_{01} + g_{02} + g_{\pi 2} + g_{m2}}{g_{02}(g_{01} + g_{\pi 2})} \right] - V_{IN} \bullet \left[\frac{g_{m1}(g_{02} + g_{m2})}{g_{02}(g_{\pi 2} + g_{01})} \right]$$
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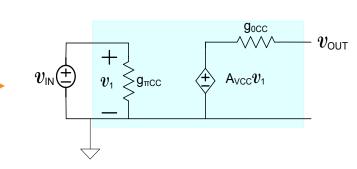
$$V_{X} = I_{X} \bullet \left[\frac{g_{01} + g_{02} + g_{\pi 2} + g_{m2}}{g_{02} (g_{01} + g_{\pi 2})} \right] - V_{IN} \bullet \left[\frac{g_{m1} (g_{02} + g_{m2})}{g_{02} (g_{\pi 2} + g_{01})} \right]$$

$$V_{IN} = I_1 \bullet \frac{1}{g_{\pi 1}}$$

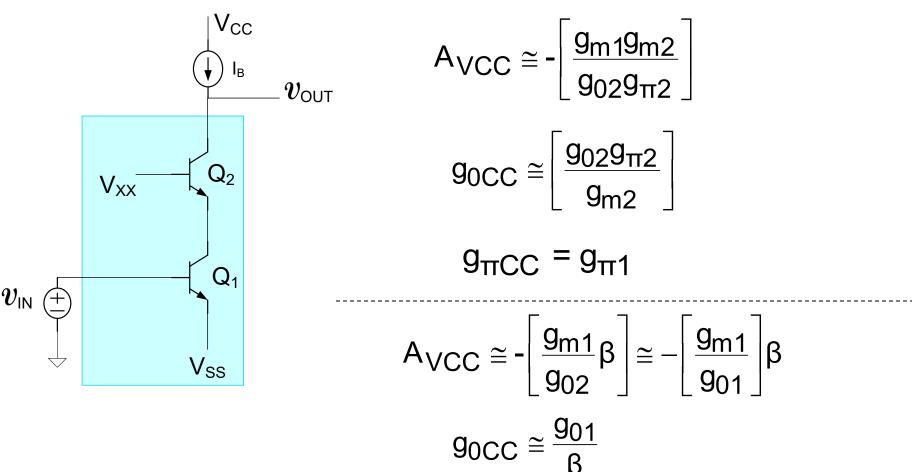
It thus follows for the npn bipolar structure that it is unilateral and :

$$A_{VCC} = - \left[\frac{g_{m1}(g_{02} + g_{m2})}{g_{02}(g_{\pi 2} + g_{01})} \right] = - \left[\frac{g_{m1}g_{m2}}{g_{02}g_{\pi 2}} \right]$$

$$g_{0CC} = \left[\frac{g_{02} \left(g_{01} + g_{\pi 2} \right)}{g_{01} + g_{02} + g_{\pi 2} + g_{m2}} \right] \cong \left[\frac{g_{02} g_{\pi 2}}{g_{m2}} \right]$$

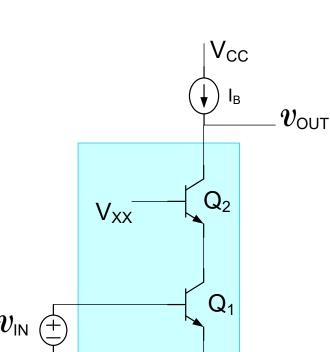






- Voltage gain is a factor of β larger than that of the CE amplifier with current source load
- Output impedance is a factor of β larger than that of the CE amplifier $_{65}$





 V_{SS}

$$A_{VCC} \cong - \left[\frac{g_{m1}}{g_{02}} \beta \right] \cong - \left[\frac{g_{m1}}{g_{01}} \right] \beta$$

$$g_{OCC} \cong \frac{g_{O2}}{\beta}$$

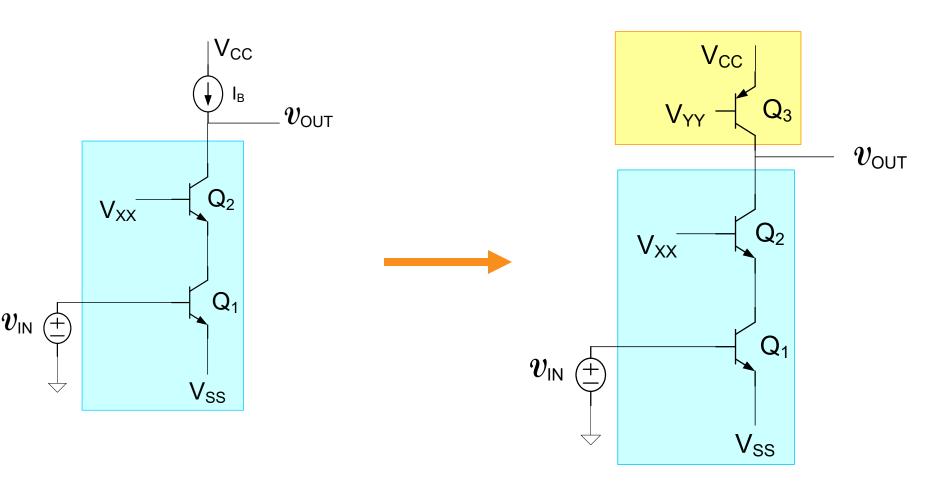
In the MPOP domain:

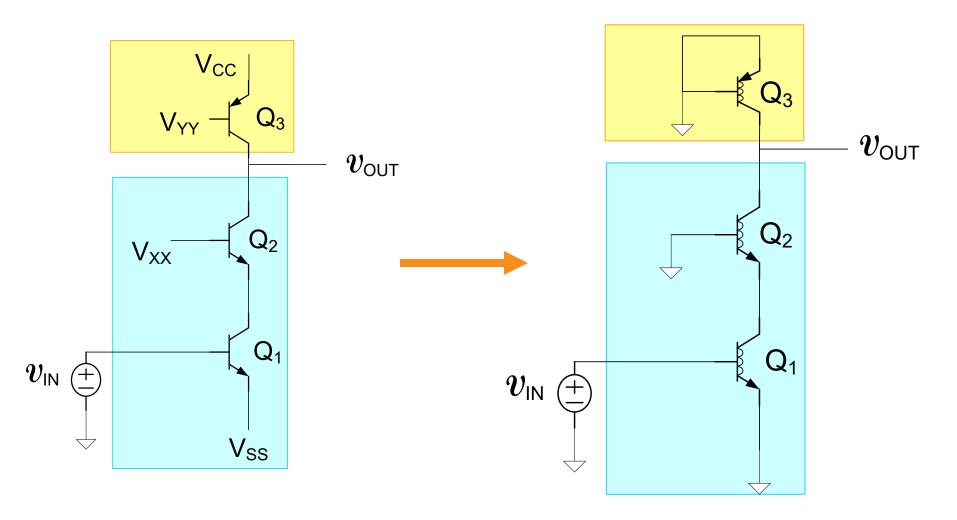
$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta = \left[\frac{2V_{AF}}{V_t}\right]\beta = \left[-8000\right]100$$

$$A_{VCC} \cong -800,000$$

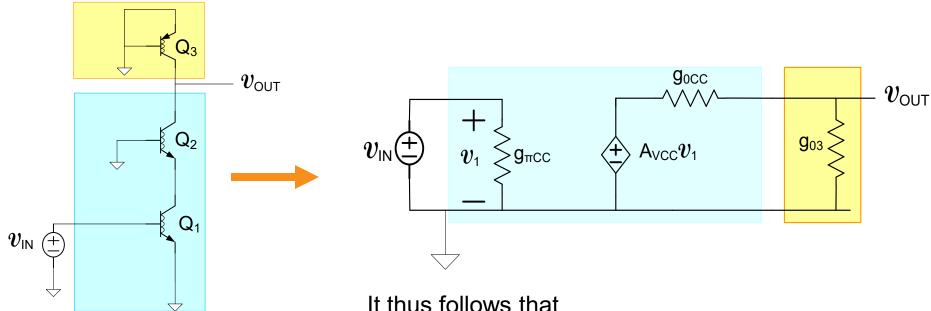
This gain is very large and only requires two transistors!

What happens to the gain if a transistor-level current source is used for I_B?





High-gain amplifier comparisons



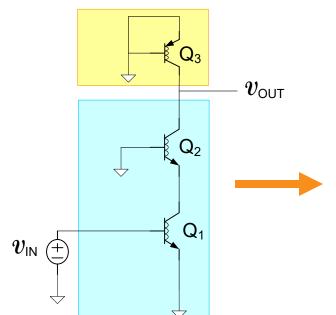
It thus follows that

$$A_{V} = A_{VCC} \left[\frac{g_{0CC}}{g_{03} + g_{0CC}} \right]$$

But
$$g_{0CC} \simeq g_{01}/\beta = g_{03}/\beta$$

$$A_{V} \cong A_{VCC} \left[\frac{g_{0CC}}{g_{03}} \right] \cong \frac{A_{VCC}}{\beta}$$

This is a dramatic reduction in gain compared to what the ideal current source biasing provided 69



$$A_{V} \cong A_{VCC} \left[\frac{g_{0CC}}{g_{03}} \right] \cong \frac{A_{VCC}}{\beta}$$

But recall

$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$

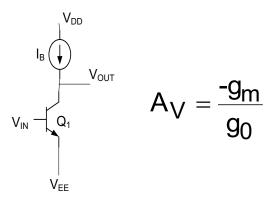
Thus
$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$

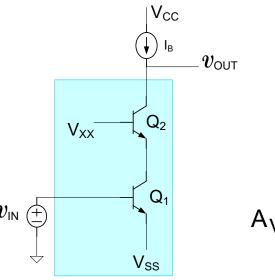
In the MPOP domain:

$$A_{V} \cong - \begin{bmatrix} I_{CQ} \\ V_{t} \\ I_{CQ} \\ V_{AF} \end{bmatrix} = - \begin{bmatrix} V_{AF} \\ V_{t} \end{bmatrix} \cong -8000$$

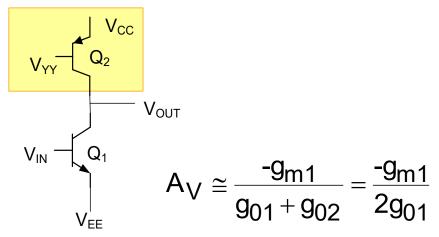
- This is still a factor of 2 better than that of the CE amplifier with transistor current source $A_{VCE} = -\left[\frac{g_{m1}}{2q_{01}}\right]$
- It only requires one additional transistor
- But its not nearly as good as the gain the cascode circuit seemed to provide $_{70}$

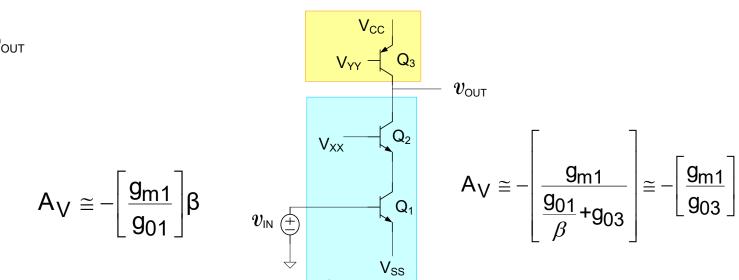
Cascode Configuration Comparisons





$$A_V \cong - \left| \frac{g_{m1}}{g_{01}} \right| \beta$$



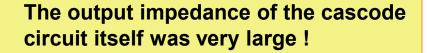


Gain limited by output impedance of current scource !!

Can we design a better current source? In particular, one with a higher output impedance?

Better current sources

Need a higher output impedance than go

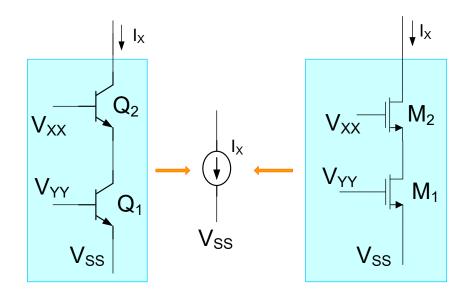




$$g_{0CC} \cong \frac{g_{01}}{\beta}$$

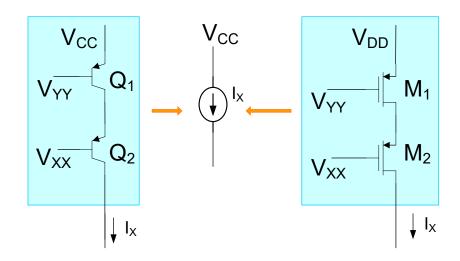
Can a current source be built with the cascode circuit?

Cascode current sources

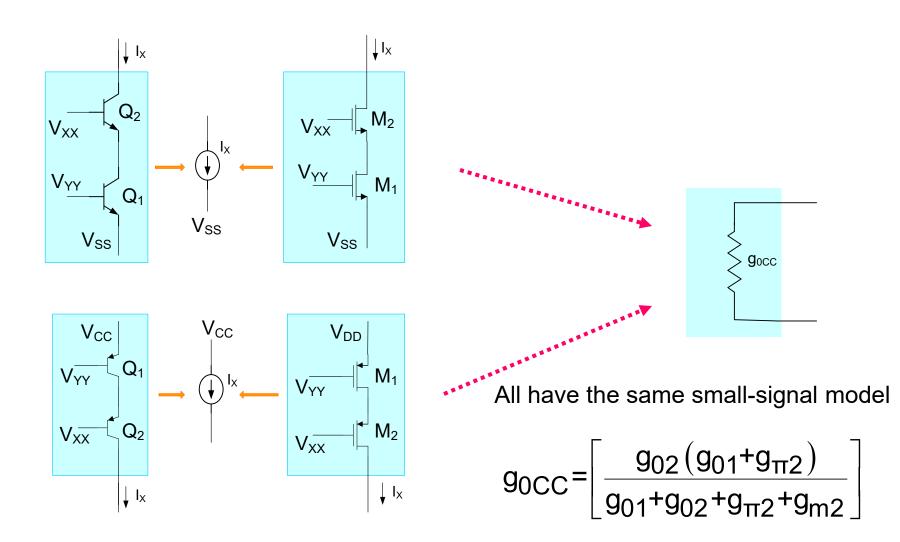




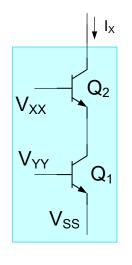


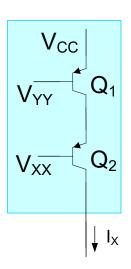


Cascode current sources



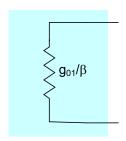
Cascode current sources

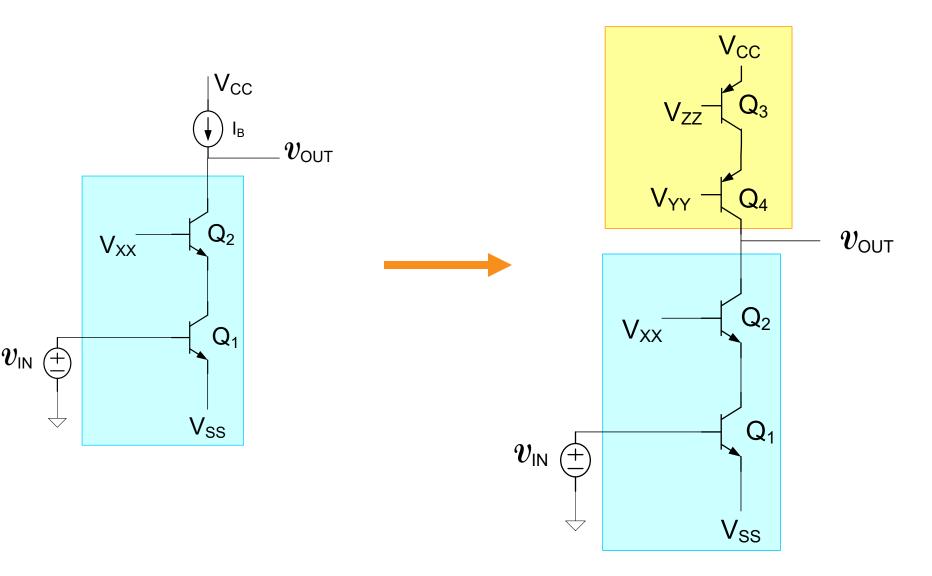




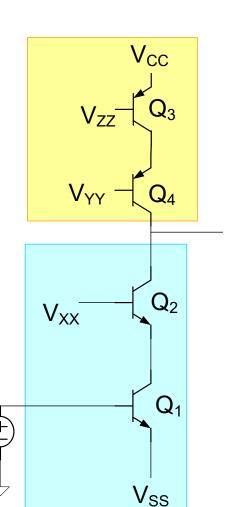
For the BJT cascode current sources

$$g_{0CC} = \left[\frac{g_{02} (g_{01} + g_{\pi 2})}{g_{01} + g_{02} + g_{\pi 2} + g_{m2}} \right] \approx \left[\frac{g_{02} g_{\pi 2}}{g_{m2}} \right] = \frac{g_{01}}{\beta}$$









 v_{IN}

 v_{out}

$$A_{V} \cong -\left[\frac{g_{m1}}{\frac{g_{01}}{\beta_{l}} + g_{0CC}}\right] \cong -\left[\frac{g_{m1}}{\frac{g_{01}}{\beta_{l}} + \frac{g_{03}}{\beta_{3}}}\right]$$

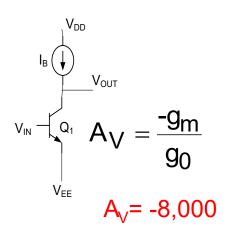
$$A_{V} = - \left[\frac{g_{m1}}{g_{01}} \right] \frac{\beta}{2}$$

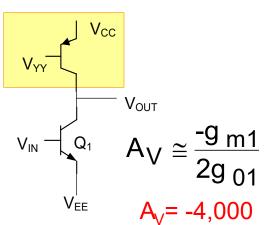
If $\beta_1 = \beta_3 = \beta$

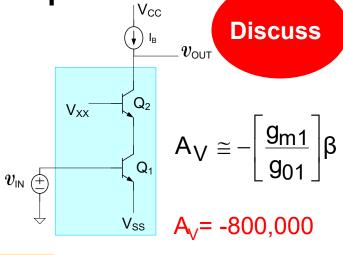
$$A_V = -[8000] \frac{100}{2} \cong -400,000$$

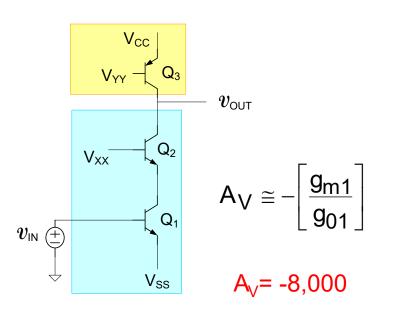
- This gain is very large and is a factor of 2 below that obtained with an ideal current source biasing
- Although the factor of 2 is not desired, the performance of this circuit is still very good
- This factor of 2 gain reduction is that same as was observed for the CE amplifier when a transistor-level current source was used
- Biasing voltages V_{ZZ} and V_{SS} are critical so seldom used single-ended but good biasing strategies exist for differential operation

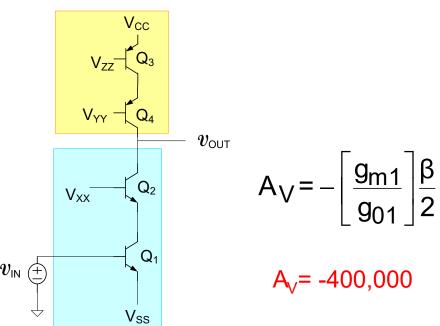
Cascode Configuration Comparisons



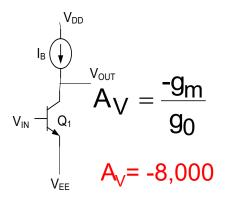


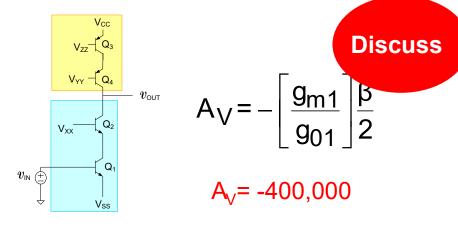


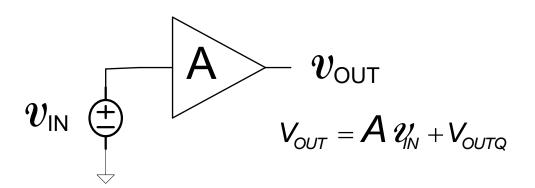




High Gain Amplifiers Seldom Used Open Loop

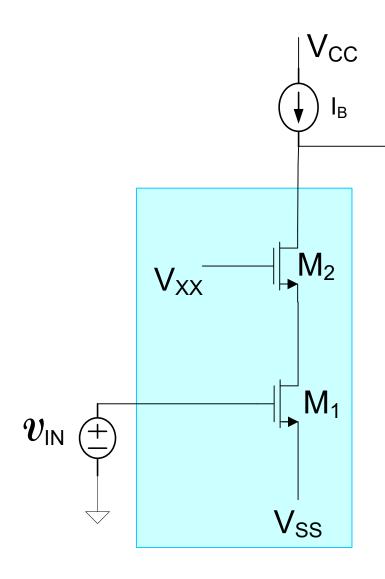






If A_V =-400,000 and V_{IN} increases by 1mV, what would happen at the output?

The Cascode Amplifier (consider n-ch MOS version)



Discuss

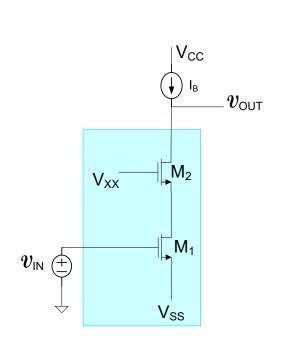
$$A_{VCC} \cong - \left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}} \right]$$

$$90CC \cong \left[\frac{901902}{9m2}\right]$$

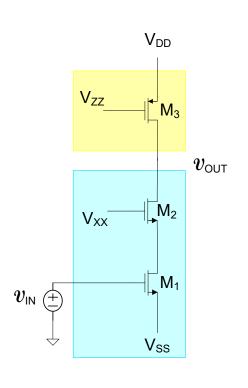
Same issues for biasing with current source as for BJT case

With cascode current source for I_B , gain only drops by a factor of 2 from value with ideal current source

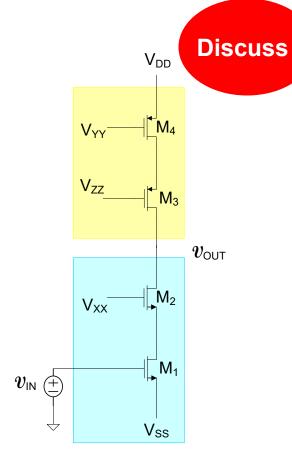
The Cascode Amplifier (consider n-ch MOS version)



$$A_{VCC} \cong - \left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}} \right]$$



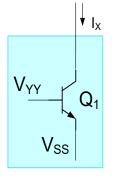
$$A_{VCC} \cong - \left[\frac{g_{m1}}{g_{01}} \right]$$

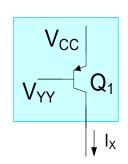


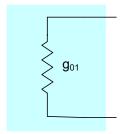
$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right] \qquad A_{VCC} \cong -\frac{1}{2}\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$

Current Source Summary (BJT)

Basic

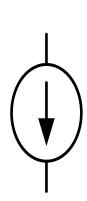


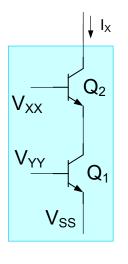


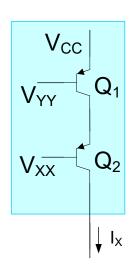


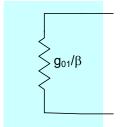
$$g_0 \cong g_{01}$$

Cascode





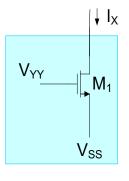


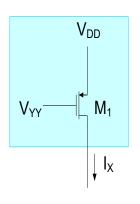


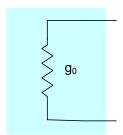
$$g_{0CC} \cong \frac{g_{01}}{\beta}$$

Current Source Summary (MOS)

Basic

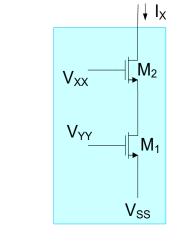


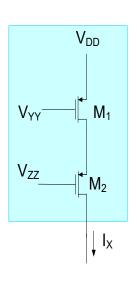


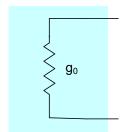


$$g_0 \cong g_{01}$$

Cascode

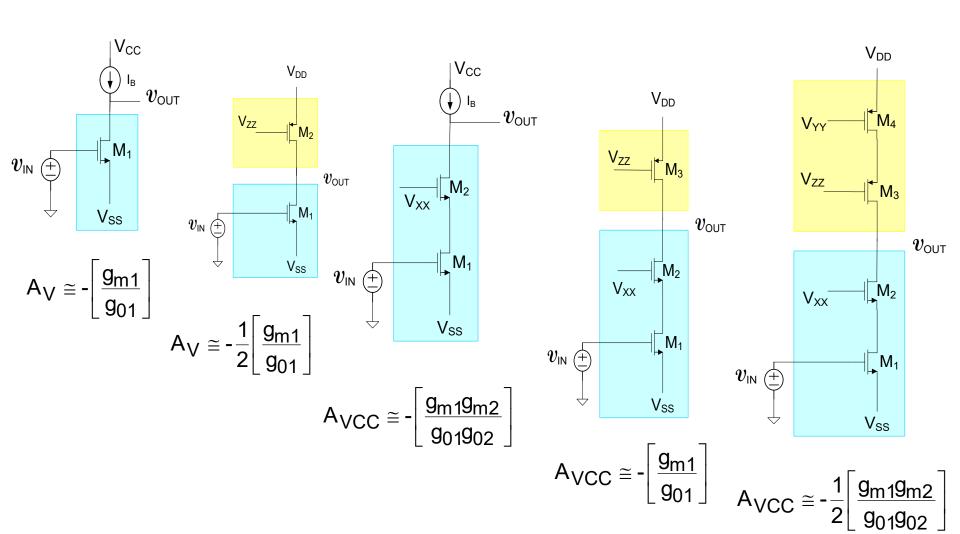






$$g_0 \cong g_{01} \frac{g_{02}}{g_{m2}}$$

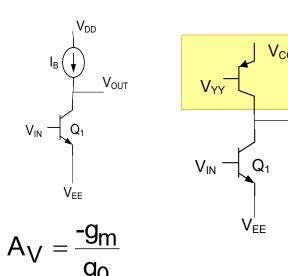
High Gain Amplifier Comparisons (n-ch MOS)



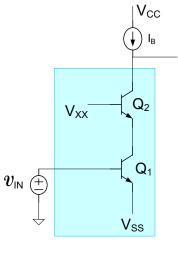
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High Gain Amplifier Comparisons (BJT)



$$A_V \cong -\frac{1}{2} \frac{g_{m1}}{g_{01}}$$

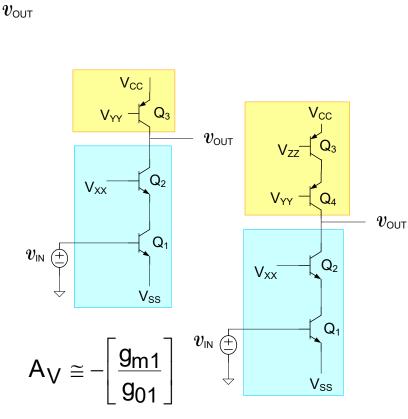


$$A_{V} \cong - \left[\frac{g_{m1}}{g_{01}}\right] \beta$$

 Single-ended high-gain amplifiers inherently difficult to bias (because of the high gain)

 V_{OUT}

- Biasing becomes practical when used in differential applications
- These structures are widely used but usually with differential inputs



$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right] \frac{\beta}{2}$$
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Stay Safe and Stay Healthy!

